REMARKS

Claims 16, 19 are amended, no claims are canceled, and claims 87-95 are added; as a result, claims 1-23 and 85-95 are now pending in this application.

§*102/103 Rejection of the Claims*

Claim 1 was rejected under 35 U.S.C. § 102(e) for anticipation by, or in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Lee (U.S. 2002/0106536). Applicant respectfully traverses this rejection.

The cited reference of Lee discloses a non-floating gate transistor having a substrate 10, with a metal silicate layer 12 formed directly on the substrate 10. The silicate layer has the form of a metal–silicon-oxide, where the metal can be Hf, Zr, Ta, Ti and Al (see [0019]). The dielectric layer 14 over the silicate layer 12 may be a high k material, or a multiple material layer. There is no disclosure of a low tunnel barrier, or of any asymmetry of the dielectric, or of an integrate insulator since there is only a single gate electrode disclosed.

Applicant respectfully submits that the cited reference does not disclose at least the claimed features of "*...a control gate opposing the floating gate; and wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator formed by multiple atomic layer deposition (ALD) ...*", as recited in independent claim 1. There is no floating gate disclosed or discussed in the reference, there are no pairs of gates opposing each other, there is no gate separated from the channel region by a gate oxide, and there is no intergate insulator, no asymmetrical intergate insulator, and no low tunnel barrier insulator. Applicant submits that the statement on page 3, last paragraph of the Office Action that the material of the insulator contacting the substrate must be different from the material contacting the gate is incorrect, since the bottom layer 18 may be Al_2O_3 and the top layer 22 is stated to be Al_2O_3 (see paragraph [0059]).

In view of the above discussion on the differences between the recited features of claim 1 and the cited reference, Applicant requests that this rejection be reconsidered and withdrawn.

Claims 1, 3, 4, and 9 were rejected under 35 U.S.C. § 102(b) for anticipation by, or in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Endo (U.S. 5,619,051). Applicant respectfully traverses this rejection.

The cited reference of Endo discloses a floating gate transistor having a gate oxide 14b on a substrate 10, and a nitride layer 14a on the oxide layer 14b. There is a floating gate 16 made of polysilicon, an intergate insulator 18 made of a high constant material, and a control gate 20 made of a layer of either ruthenium oxide or indium oxide and covered with a layer of titanium nitride, palladium or platinum (col. 4, lines 1-5).

Applicant respectfully disagrees with the statement on page 5 of the Office Action, that there is "an explicit description of a 0.4 eV difference in barrier heights between the two surfaces", when the indicated portion of the reference, column 7, last paragraph is that "In barium titanate the forbidden band width is about 3.0 eV, and in strontium titanate that is about 3.4 eV", which is believed to discuss the difference between the valence level and the conduction level (see for example Applicant's figure 7A and col. 17, lines 23) and is not directly connected to the tunnel barrier height, which is the difference between the Fermi level and the conduction level. Thus Applicant submits that the tunnel barrier height is not disclosed or discussed in the cited reference of Endo, and that the use of ALD to form insulator layers that do not react with the electrodes to form interface materials (see Applicant's specification at page 21 line 27) due to the lower deposition temperatures with ALD as compared to CVD operations, and thus does provide a different structure that has patentable weight.

Specifically, Applicant respectfully submits that the cited reference does not disclose at least the claimed features of "*...a control gate opposing the floating gate; and wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator formed by multiple atomic layer deposition (ALD)* ...", as recited in independent claim 1, from which claims 3, 4 and 9 depend, either directly or indirectly. The cited reference does not disclose anything regarding asymmetrical oxides, or suggest that there is any problem with the disclosed CVD insulators, and thus there can be no motivation for one of ordinary skill to use the cited reference to change the disclosed arrangement to obtain the asymmetrical insulator formed by ALD of the claimed invention. Applicant requests that this rejection be reconsidered and withdrawn.

§103 Rejection of the Claims

Claims 10, 11, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo in view of Orlowski et al. (U.S. 6,433,382). Applicant respectfully traverses this rejection.

The cited reference of Endo has been discussed above. The cited reference of Orlowski is used in the outstanding Office Action to show that vertical non volatile transistors are known in the art.

Applicant respectfully submits that Orlowski does nothing to cure the failures of the Endo reference to disclose the features of asymmetrical intergate insulators, as discussed above with reference to the previous rejection of claim 1. Specifically, the suggested combination of reference does not describe or suggest at least the combination of features of "*...wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator, formed by atomic layer deposition (ALD) having a number of small compositional ranges such that gradients can be formed which produce different barrier heights at an interface with the floating gate and control gate ...*", as recited in claim 10, from which claims 11, 14 and 15 depend, either directly or indirectly. Neither reference has any disclosure or suggestion of using an asymmetrical insulator to change the low tunneling barrier height, which is also not described or suggested in either reference, at the control gate versus the floating gate. Applicant requests that this rejection be reconsidered and withdrawn.

Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo as applied to claim 1 above, and further in view of Eguchi et al. (U.S. 5,618,761). Applicant respectfully traverses this rejection.

The cited reference of Endo has been discussed above. The cited reference of Eguchi is used in the outstanding Office Action to show that insulators having a Perovskite composition are known in the art.

Applicant respectfully submits that Orlowski does nothing to cure the failures of the Endo reference to disclose the use of ALD and asymmetrical intergate insulators, as discussed above with reference to the rejection of claim 1, from which claims 5 and 6 depend.

Specifically, Applicant respectfully submits that the suggested combination of references do not disclose at least the claimed features of "*...a control gate opposing the floating gate; and wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator formed by multiple atomic layer deposition (ALD) ...*", as recited in independent claim 1. In view of the above discussion, Applicant requests that this rejection be reconsidered and withdrawn.

Claims 7-8, 12-13, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo. Applicant respectfully traverses this rejection.

The cited reference of Endo has been discussed above, and Applicant again submits that the asymmetrical intergate insulator is not discussed, disclosed or suggested in the Endo reference. Endo is concerned with having the dielectric film between the floating gate and the control gate formed of at least two layers, where the permittivity of the second layer is at least 13 times higher than the permittivity of the first layer (see col. 2, lines 22 – 38; col. 10, line 9). The Endo reference has no disclosure or suggestion that Applicant can find having anything to do with asymmetric insulators or with ALD depositions.

Specifically, claim 1 recites "*...a control gate opposing the floating gate; and wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator formed by multiple atomic layer deposition (ALD) ...*", which is not described or suggested by the Endo reference, whether taken alone or in any combination with other well known art. Claims 7 and 8 depend from claim 1, and are thus believed to be in patentable condition. Claim 7 is further believed to be patentable over Endo because the recited "*...polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator ...*", is not found or suggested by Endo. Endo has the intergate insulator 18 in direct contact with the floating gate polysilicon 16 and with the control gate 20 ruthenium oxide or indium oxide (see col. 4, lines 1-5). Claim 8 is further believed to be patentable over Endo because the recited "*... control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a*

different work function than the metal layer formed on the floating gate ...", is not suggested by Endo for the same reasons just given with respect to claim 7.

Claims 12 and 13 recite similar limitations over independent claim 10, as those discussed above. The Endo reference clearly does not describe or suggest having metal layers between the intergate insulator and the gates, and thus does not suggest the claimed arrangement.

Claim 18 recites "*...a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide; a first metal layer formed on the polysilicon floating gate; a metal oxide intergate insulator formed by atomic layer deposition on the metal layer, wherein the metal oxide intergate insulator includes an asymmetrical metal oxide having a number of small compositional ranges such that gradients can be formed in an applied electric field which produce different barrier heights at an interface with the floating gate and control gate; a second metal layer formed on the metal oxide intergate insulator, wherein the second metal layer has a different work function from the first metal layer; and a polysilicon control gate formed on the second metal layer...*", which is not described or suggested by the Endo reference, whether taken alone or in any combination with other well known art. Endo does not show, suggest, or discuss the use of a first metal layer formed on the floating gate in contact with the intergate insulator, or a second metal layer formed on the intergate insulator, and surely does not suggest that the metal layers have different work functions.

In view of the above noted differences between the cited Endo reference and the claimed invention, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claim 23 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo as applied to claim 18 above, and further in view of Orlowski et al. Applicant respectfully traverses this rejection.

The cited references of Endo and Orlowski have features that have been discussed above. Orlowski is used in the outstanding Office Action to show that vertical non volatile transistors are known in the art. Claim 18, from which claim 23 depends, recites "*...a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide; a first metal layer formed on the polysilicon floating gate; a metal oxide intergate insulator formed by atomic layer deposition on the metal layer, wherein the metal oxide intergate insulator includes an*

asymmetrical metal oxide having a number of small compositional ranges such that gradients can be formed in an applied electric field which produce different barrier heights at an interface with the floating gate and control gate; a second metal layer formed on the metal oxide intergate insulator, wherein the second metal layer has a different work function from the first metal layer; and a polysilicon control gate formed on the second metal layer...", which is not described or suggested by the Endo reference, whether taken alone or in any combination with Orlowski. Endo does not suggest a first metal layer formed on the floating gate in contact with the intergate insulator, or a second metal layer formed on the intergate insulator, or that the metal layers have different work functions. In view of the above noted differences between the cited Endo reference and the claimed invention, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claims 10, 11, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo in view of Shinkawata et al. (U.S. 2002/0008324). Applicant notes that the body of the rejection refers to claims 2, 20-22, and 85-86, and will response to the specific rejection arguments given in the Office Action. Applicant respectfully traverses this rejection.

Endo has been discussed above, and Shinkawata is used in the outstanding Office Action to show that Al_2O_3 is equivalent to $SrTiO_3$.

Applicant respectfully submits that Shinkawata does nothing to cure the above noted failures of the Endo reference to disclose or suggest asymmetrical intergate insulators, or low tunnel oxide barrier or the use of ALD to form the intergate insulator, as discussed above with reference to the previous rejection of claim 10. Specifically, the suggested combination of reference does not describe or suggest at least the combination of features of "*...wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator, formed by atomic layer deposition (ALD) having a number of small compositional ranges such that gradients can be formed which produce different barrier heights at an interface with the floating gate and control gate ...*", as recited in claim 10, from which claims 11, 14 and 15 depend, either directly or indirectly. Neither reference discloses or suggests of an asymmetrical intergate insulator, or a low tunneling barrier height, or ALD deposition. As noted above, ALD depositions result in a physically different interface structure, and the claimed

properties can not be obtained using the disclosed methods of Endo. In light of the above, Applicant requests that this rejection be reconsidered and withdrawn.

Allowable Subject Matter

Claims 16-17 and 19 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has rewritten claims 16-17 and 19 in accordance with the Examiner's suggestion. The rewriting of these claims does not narrow the claim scope. These claims are not amended in view of any substantive rejection. Applicant requests that claims 16-17 and 19 be allowed with new dependent claims 87-95.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29 day of July, 2005.

KACIA LEE _____ Kacia Lee

Name Signature